Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A non-volatile content addressable memory, comprising:

a multiplicity of memory cells ordered into a matrix of rows and columns;

a word line associated with every row of cells;

a first and a second bit line associated with every column of cells;

an input terminal and an output terminal;

a ground control line, a ground line and a match control line associated with every row of cells;

a search activation terminal and a match indication terminal associated with every row of cells;

each cell comprising:

a first non-volatile memory element having a control terminal connected to the word line associated with the row containing the cell, a first terminal connected to the first bit line associated with the column containing the cell and a second terminal connected to a match node of the cell;

a second non-volatile memory element having a control terminal connected to the word line associated with the row containing the cell, a first terminal connected to the second bit line associated with the column containing the cell and a second terminal connected to the match node of the cell;

a first controlled electronic switch connected between the input terminal and the output terminal of the cell and having a control terminal connected to the match node of the cell, the controlled electronic switches of the cells of the same row being connected in series with each other between the search activation terminal and the match indication terminal associated with the row;

a second controlled electronic switch connected between the ground line associated with the row containing the cell and the cell output terminal and having a control terminal connected to the match control line associated with the row containing the cell; and

a third controlled electronic switch connected between the match node of the cell and the ground line associated with the row containing the cell and having a control terminal connected to the ground control line associated with the row containing the cell.

2. (Original) The content addressable memory of claim 1 wherein the first and the second non-volatile memory element of each cell are transistors of the floating-gate type in which the first terminal is the drain and the second terminal is the source, and the first, the second and the third controlled electronic switches of each cell are MOS transistors.

3. (Original) The content addressable memory of claim 1 wherein each row of cells comprises at least a buffer between the search activation terminal and the match indication terminal.

4. (Original) The content addressable memory of claim 1, in each cell of which:

when the first non-volatile memory element has a low threshold voltage and the second non-volatile memory element has a high threshold voltage, there is memorized a logic 1;

when the first non-volatile memory element has a high threshold voltage and the second non-volatile memory element has a low threshold voltage, there is memorized a logic 0; and

when both the non-volatile memory elements have low threshold voltages, there is memorized a don't care state X.

Claims 5.-9. (Canceled)

10. (Original) A content addressable memory, comprising:

a plurality of memory cells arranged in a matrix of rows and columns and having a word line associated with every row and first and second bit lines associated with every column;

an input terminal and an output terminal;

a ground control line, a ground line, a match control line, a search activation terminal, and a match indication terminal associated with every row of cells;

the matrix of memory cells configured to generate a match signal whenever a voltage on the match indication terminal varies, and generating a no-match signal when a voltage on the match indication terminal does not vary.

11. (Original) A memory cell for a content addressable memory, the cell comprising:

a first non-volatile memory element having a control terminal connected to word line associated with the cell, a first terminal connected to a first bit line associated with the cell, and a second terminal connected to a match node of the cell;

a second non-volatile memory element having a control terminal connected to the word line, a first terminal connected to a second bit line associated with the cell, and a second terminal connected to the match node of the cell;

a first controlled electronic switch connected between an input terminal associated with the memory cell and an output terminal associated with the memory cell, the first controlled electronic switch having a control terminal connected to the match node, the first controlled electronic switch configured to be coupled in series in a row of memory cells between a search activation terminal and a match indication terminal associated with the row;

a second controlled electronic switch connected between a ground line associated with the cell and the output terminal, and further having a control terminal configured for connection to a match control line associated with the row in which the cell is coupled; and

a third controlled electronic switch coupled between the match node and the ground line, and further having a control terminal configured for connection to a ground control line associated with the row in which the cell is configured to be coupled.

12. (Original) The memory cell of claim 11 wherein the first and the second non-volatile memory element each comprise a transistor of the floating-gate type in which the first terminal is the drain and the second terminal is the source.

13. (Original) The memory cell of claim 12 wherein the first, second, and third controlled electronic switches of the cell comprise MOS transistors.

14. (Original) The memory cell of claim 11 wherein the first and second transistors are configured such that:

when the first transistor has a low threshold voltage and the second transistor has a high threshold voltage, there is stored therein a logic 1;

when the first transistor has a high threshold voltage and the second transistor has a low threshold voltage, there is stored therein a logic 0; and

when the first and second transistors each have low threshold voltages, there is stored therein a don't care state.

15. (Canceled)

16. (Withdrawn) A memory, comprising:

a plurality of memory cells arranged in rows and columns forming a memory matrix, each memory cell comprising:

a first transistor having a control gate coupled to a word line, a first terminal coupled to a first bit line, and a second terminal coupled to a first node;

a second transistor having a control gate coupled to the word line, a first terminal coupled to a second bit line, and a third terminal coupled to the first node;

a third transistor having a control gate coupled to a control line, a first terminal coupled to the first node, and a second terminal coupled to a voltage reference source;

a fourth transistor having a control gate coupled to a match control line, a first terminal coupled to the voltage reference source, and a second terminal coupled to a match output line; and

a fifth transistor having a control gate coupled to the first node, a first terminal coupled to the match output line, and a second terminal coupled to a match input line.

17. (Withdrawn) The memory of claim 16 wherein the first and second transistors comprise field effect transistors.

18. (Withdrawn) A computer system, comprising:

a microprocessor having a memory associated therewith, the memory comprising:

a plurality of memory cells arranged in rows and columns forming a memory matrix, each memory cell comprising:

a first transistor having a control gate coupled to a word line, a first terminal coupled to a first bit line, and a second terminal coupled to a first node;

a second transistor having a control gate coupled to the word line, a first terminal coupled to a second bit line, and a third terminal coupled to the first node;

a third transistor having a control gate coupled to a control line, a first terminal coupled to the first node, and a second terminal coupled to a voltage reference source;

a fourth transistor having a control gate coupled to a match control line, a first terminal coupled to the voltage reference source, and a second terminal coupled to a match output line; and

a fifth transistor having a control gate coupled to the first node, a first terminal coupled to the match output line, and a second terminal coupled to a match input line.

19. (Withdrawn) The computer system of claim 18 wherein the first and second transistor comprise field effect transistors.

20. (Withdrawn) The computer system of claim 18 wherein each memory cell is configured such that:

when the first transistor has a low threshold voltage and the second transistor has a high threshold voltage, there is stored therein a logic 1;

when the first transistor has a high threshold voltage and the second transistor has a low threshold voltage, there is stored therein a logic 0; and

when the first and second transistors each have low threshold voltages, there is stored therein a don't care state.